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L7: Entry 4 of 27 File: PGPB Feb 21, 2002

DOCUMENT-IDENTIFIER: US 20020023242 A1
TITLE: Method and apparatus for monitoring microcomputer in electronic control unit

Abstract Paragraph:
In an electronic control unit for an anti-lock brake control system, a microcomputer communicates data to a peripheral IC. The peripheral IC monitors a fault of the microcomputer based on data received from the microcomputer. The monitoring operation may be executed by measuring an interval of calculation, calculation result and sequence of data transmitted from the microcomputer.

Summary of Invention Paragraph:
[0002] The present invention relates to a method and apparatus for monitoring a microcomputer provided in an electronic control unit.

Summary of Invention Paragraph:
[0003] A microcomputer provided in an electronic control unit (ECU) for vehicles is generally monitored to detect whether the microcomputer is functioning normally or not, whether an input to the microcomputer is normal or not, or whether arithmetic operation in the microcomputer is carried out accurately or not.

Summary of Invention Paragraph:
[0004] The monitoring is conducted, for example, by executing the watch-dog (WD) monitoring to detect whether the arithmetic calculation period in a monitoring integrated circuit (IC) is in the correct period or not by inputting the arithmetic calculation period to the monitoring IC from the microcomputer. It may also be conducted by comparing the arithmetic calculation result of each microcomputer by using additional microcomputer of the same structure as the microcomputer to conduct the arithmetic calculation operation.

Summary of Invention Paragraph:
[0005] However, the WD monitoring results in that the monitoring capability is insufficient because contents of monitoring are limited. The mutual monitoring using a couple of microcomputers results in that a fault cannot be detected if there is an error in data inputted to a couple of microcomputers and that monitoring cost becomes high because a couple of microcomputers are used.

Summary of Invention Paragraph:
[0006] It is therefore an object of the present invention to provide a method of monitoring a microcomputer without requiring a couple of microcomputers.

Summary of Invention Paragraph:
[0007] According to the present invention, a microcomputer and a peripheral IC are connected to communicate data with each other. The peripheral IC monitors a fault of the microcomputer based on the data received from the microcomputer. The monitoring operation may be executed by measuring an interval of calculation, calculation result and sequence of data transmitted from the microcomputer. The microcomputer monitors a fault of the peripheral IC based on the data received from the peripheral IC.

Brief Description of Drawings Paragraph:

[0012] FIG. 4A is a circuit diagram illustrating an interval monitoring logic circuit, and

Brief Description of Drawings Paragraph:
[0014] FIG. 5A is a circuit diagram illustrating a microcomputer fault monitoring logic circuit, and

Brief Description of Drawings Paragraph:
[0016] FIG. 6A is a circuit diagram illustrating a microcomputer fault monitoring logic circuit for the ABS control, and

Brief Description of Drawings Paragraph:
[0018] FIG. 7A is a circuit diagram illustrating a sequence monitoring logic circuit, and

Brief Description of Drawings Paragraph:
[0020] FIG. 8 is a circuit diagram illustrating a wheel speed calculation monitoring circuit according to a second embodiment of the present invention; and

Brief Description of Drawings Paragraph:
[0021] FIG. 9A is a circuit diagram illustrating a microcomputer fault monitoring logic circuit for a brake assisting control, and

Detail Description Paragraph:
[0023] The present invention will be described in detail with reference to embodiments, which are directed to an electronic control unit (ECU) for vehicles.

Detail Description Paragraph:
[0032] FIG. 2 illustrates a block diagram illustrating the internal structure of the ABS control ECU 50. As illustrated in this figure, the ABS control ECU 50 has a plurality of chips including a microcomputer 60, a peripheral IC 70, a solenoid driver 90 and a semiconductor relay 100 or the like.

Detail Description Paragraph:
[0033] Details of each structural device of the ABS control ECU 50 will then be described. Each arrow mark in a solid line in FIG. 2 indicates a control system line, each arrow mark in a broken line indicates a monitor system line, and each arrow mark in a chain line indicates an inhibit/shut-off system line. The control system line means that a device at the front end of the arrow mark is controlled based on a signal from a device at the rear end of the arrow mark. Moreover, the monitor system line means that a device at the front end of the arrow mark monitors whether a specified device fails or not based on a signal from a device at the rear end of the arrow mark. Moreover, the inhibit/shut-off system line means that a device at the front end of the arrow mark inhibits or shuts off a drive of a specified device based on an inhibit/shut-off signal from a device at the rear end of the arrow mark.

Detail Description Paragraph:
[0035] Next, the peripheral IC 70 comprises a wheel speed input buffer 71, a switch (SW) signal input buffer 72, a serial communication buffer 73, a serial communication monitoring unit 74, an internal oscillator circuit 75, a watch-dog (WD) monitoring unit 76, a reset control unit 77, a drive inhibit signal generating unit 78, a relay drive unit 79, a lamp drive circuit 80, an excessive-heating protection circuit 81, a power supply monitoring unit 82, a power supply output circuit 83, a signal input/output buffer 84 and a temperature monitoring unit 85. Each device circuit or unit is integrated into one chip to form the peripheral IC 70.

Detail Description Paragraph:
[0037] The SW signal input buffer 72 monitors ON/OFF signal of the stop switch 29

and a signal indicating that the power is fed or not to the solenoids of the dual-position valves 21 to 24, 31 to 34 (for example, a voltage value applied on the solenoid) indicated in FIG. 1. Thereby, the ON/OFF signal indicating whether the brake pedal 27 is stepped on or not and the ON/OFF signal indicating whether the electric power is supplied to the solenoid or not can be outputted.

Detail Description Paragraph:
[0039] The serial signal monitoring unit 74 monitors the microcomputer 60 based on the serial signal from the serial communication buffer 73. More specifically, the serial communication buffer 73 receives the result of arithmetic operation from the microcomputer 60 based on the signals from the wheel speed input buffer 71 and SW signal input buffer 72 to monitor whether this signal is normal or not. For example, when the signal indicating the ABS control condition is transmitted from the serial control unit 64 in spite that the OFF signal indicating that the stop switch 29 is not stepped on is transmitted from the SW signal input buffer 72, it is determined that the serial signal from the microcomputer 60 is not normal. When the serial signal from the microcomputer 60 is not normal, a reset signal is outputted to the reset control unit 77 described later or an inhibit signal is transmitted to the drive inhibit signal generating circuit 78.

Detail Description Paragraph:
[0040] The internal oscillator unit 75 forms an internal clock used in the serial signal monitoring unit 74 and the WD monitoring unit 76 or the like. In this internal oscillator unit 75, a plurality of clock signals are generated at different time points (timings) and the serial signal monitoring unit 74 and WD monitoring unit 76 select the clock signal of appropriate timing as a monitor signal to realize a monitoring function.

Detail Description Paragraph:
[0041] The WD monitoring unit 76 monitors whether the arithmetic operation in the microcomputer 60 is performed normally or not based on the data such as arithmetic operation period produced from the microcomputer 60. For example, since the WD monitor signal is produced as a signal that is alternately inverted when the arithmetic operation is performed normally, if the WD monitor signal is not inverted alternately, it indicates that the arithmetic operation of the microcomputer 60 is not executed normally. When the arithmetic operation of the microcomputer 60 is not executed in the normal period, a reset signal is outputted to the reset control unit 77 described later or the inhibit signal is transmitted to the drive inhibit signal generating circuit 78.

Detail Description Paragraph:
[0042] At the time of initialization or when the reset signal is inputted to the reset control unit 77 from the serial signal monitoring unit 74, WD monitoring unit 76 and power supply monitoring unit 83 described later, the reset signal is transmitted to the microcomputer 60. Upon reception of this reset signal, the microcomputer 60 sets the values thereof to a mode of a predetermined reset condition. For example, the microcomputer 60 stops all arithmetic operations. Moreover, this reset signal is also transmitted to the serial communication buffer 73 and serial signal monitoring unit 74 for the purpose of initialization based on this reset signal.

Detail Description Paragraph:
[0043] The drive inhibit signal generating unit 78 transmits a solenoid drive inhibit signal and a motor drive inhibit signal to the relay drive unit 79 based on the inhibit signals from the serial signal monitoring unit 74, the WD monitoring unit 76, the excessive-heating protection circuit 81 and power supply monitoring unit 83 described later and also transmits directly the drive inhibit signal to a solenoid drive driver 90 without via the microcomputer 60. Therefore, when the solenoid drive inhibit signal is transmitted from the drive inhibit signal generating unit 78, the drive of solenoids is inhibited even when the microcomputer

60 is in operation.

Detail Description Paragraph:
[0044] The relay drive unit 79 controls switching of a semiconductor relay unit 100 and also controls power supply to the motor to drive the solenoids and pumps 45a, 45b based on the solenoid drive signals and motor drive signal from the microcomputer 60. Moreover, when the solenoid drive inhibit signal and motor drive inhibit signal are inputted from the drive inhibit signal generating unit 78 and the output monitoring unit 92 of the solenoid driver 90, the relay drive unit 79 stops power supply to the solenoids and to the motor with the semiconductor relay unit 100.

Detail Description Paragraph:
[0047] The power supply output circuit 82 corresponds to a monitored block and is connected to a power supply terminal (first power supply terminal) 101 and a ground terminal (first ground terminal) connected to an external power supply allocated at the outside of the ECU 50. The power supply output circuit 82 outputs a predetermined voltage (for example, 5V, 3.3V) based on the voltage applied to the power supply terminal 101. An output voltage of the power supply output circuit 82 is used as a power supply voltage of the microcomputer 60, the peripheral IC 70 and the solenoid driver 90 or the like.

Detail Description Paragraph:
[0048] The power supply monitoring unit 83 corresponds to a monitor block and is connected to a power supply terminal (second power supply terminal) 105 other than the power supply terminal 101 connected with the power supply output circuit 82 and a ground terminal (second power supply terminal). The power supply monitoring unit 83 monitors whether the output voltage of the power supply output circuit 82 is the predetermined value or not and also monitors whether the voltage applied to the power supply output circuit 82 is an excessive voltage or not. For example, when the output voltage of the power supply output circuit 82 is less than the predetermined voltage, a reset signal is transmitted to the reset control unit 77. When it is higher than the predetermined value, an inhibit signal is transmitted to the drive inhibit signal generating unit 78. Moreover, the voltage applied to the power supply output circuit 82 is excessive, the inhibit signal is outputted to the drive inhibit signal generating unit 78 and supplying of voltage to the microcomputer 60 is stopped to prevent excessive-heating.

Detail Description Paragraph:
[0049] The signal input/output buffer 84 is connected to a terminal 84a for checking for diagnosis when a car has a failure and makes communication with the microcomputer 60 by connecting a tester to the terminal 84a. Moreover, the signal input/output buffer 84 may be used as only an output buffer, for example, as a buffer which outputs the signal for indicating a vehicle speed displayed on a vehicle speed meter (for example, a signal corresponding to the estimated vehicle speed calculated from the wheel speed).

Detail Description Paragraph:
[0050] The temperature monitoring unit 85 always detects temperature of the ECU 50. The temperature monitoring unit 85 outputs the signal depending on the temperature of ECU 50 to the microcomputer 60 as a temperature detection signal. Based on this temperature detection signal, the microcomputer 60 performs the arithmetic operation for the ABS control depending on the detected temperature.

Detail Description Paragraph:
[0051] The solenoid driver 90 comprises MOS transistors 91 connected to the solenoids, output monitoring units 92 for monitoring voltage supply condition to the solenoids (MOS transistors 91) and AND circuits 93 for ON/OFF drive of the MOS transistors 91. The MOS transistors 91 are connected to the respective solenoids of the various control valves 21 to 24, 31 to 34 illustrated in FIG. 1 to execute

switching for voltage supply.

Detail Description Paragraph:
[0052] The output monitoring units 92 are provided on one-to-one basis to the solenoids to monitor a drive output to each solenoid. For example, it monitors the voltage supply condition to the solenoid based on the drain voltage and drain current of the MOS transistor 91. Thereby, for example, it is detected whether a drain current is excessive or not and whether a power supply wire to the solenoid is open or not or the current is leaking or not, and moreover whether the MOS transistor 91 is in the excessively high temperature or not. Thereby, if the result not suitable for driving the solenoid is attained, the output monitoring unit 92 transmits the solenoid drive inhibit signal and the motor drive inhibit signal to the relay drive unit 79 and also outputs the solenoid drive inhibit signal to the AND circuit 93.

Detail Description Paragraph:
[0053] To the AND circuit 93, an output signal of the microcomputer 60, an output signal from the relay drive unit 79, an output signal from the drive inhibit signal generating unit 78 and an output signal from the output monitoring unit 92 are inputted. In the case of this embodiment, the output signals from the relay drive unit 79, the drive inhibit signal generating unit 78 and the output monitoring unit 92 are normally at low level. However, if any failure occurs, it turns to high level and the output of the AND circuit 93 becomes low, that is, the MOS transistor 91 turns off.

Detail Description Paragraph:
[0054] Thus, the solenoid driver 90 not only shuts off the power supply to the solenoid based on the signal from the microcomputer 60 and peripheral IC 70 but also shuts off the power supply to the solenoid based on the signal from the output monitoring unit 92 provided within the solenoid driver 90 itself.

Detail Description Paragraph:
[0055] In the semiconductor relay unit 100, the power supply to the solenoids is switched by a semiconductor relay 100a, while the power supply to the motor to drive the pumps 45a, 45b is switched by a semiconductor relay 100b. These semiconductor relays 100a, 100b are constructed to be controlled on the basis of the signal from the relay drive unit 79 to normally enable power supply to the solenoids and the motors and to disable the power supply to the solenoids and the motors upon reception of the solenoid drive inhibit signal and the motor drive inhibit signal from the relay drive unit 79.

Detail Description Paragraph:
[0063] As described above, the serial signal SCI transmitted from the microcomputer 60 is received by the serial communication buffer 73 and various signals depending on this received data are outputted to the serial signal monitor unit 74 from the serial communication buffer 73.

Detail Description Paragraph:
[0066] The serial signal monitor unit 74 is shown in FIG. 4A to FIG. 7A. The logic circuit illustrated in FIG. 4A is an interval monitoring logic circuit for monitoring a processing interval in the microcomputer 60.

Detail Description Paragraph:
[0072] As described above, it is possible to monitor the interval of the arithmetic operations in the microcomputer 60 using the logic circuit illustrated in FIG. 4A.

Detail Description Paragraph:
[0073] The logic circuit illustrated in FIG. 5A is one of the arithmetic operation result monitoring logic circuits for monitoring the result of arithmetic operations in the microcomputer 60. Here, it is monitored whether the dual-position valves 21

to 24, 31 to 34 for the wheels 1 to 4 (control wheels) as the ABS control object are normally driven or not.

Detail Description Paragraph:
[0093] In this logic circuit, the period Tb is set shorter than the period Ta to immediately inhibit an output of the solenoid drive driver 90 because a fault is surely found in the arithmetic operation result of the microcomputer 60 when the solenoid drive signal is outputted in the period Tb even not in the ABS control condition. As described above, it is now possible to monitor the arithmetic operation result of the microcomputer using the logic circuit illustrated in FIG. 5A.

Detail Description Paragraph:
[0094] A logic circuit illustrated in FIG. 6A is also one of the arithmetic operation result monitoring logic circuits for monitoring the arithmetic operation result of the microcomputer 60. Here, it is monitored whether the pressure decreasing control valves 31 to 34 for the control wheel under the ABS control are driven normally or not. Namely, even during the ABC control condition, if the pressure decreasing time is too long, a driver feels, even when the driver steps the brake pedal down, a fear for insufficient effectiveness of the brake. Therefore, if the pressure decreasing time is too long, it is defined as the microcomputer 60 is in the fault condition.

Detail Description Paragraph:
[0098] As illustrated in FIG. 6B, when the pressure decreasing period is in the normal length (shorter than the period T.sub.G in the figure), the output signal CRES of the OR circuit 502 becomes high level and the signal f$$RF does not become high level before the counter 501 counts up to the final digit. Meanwhile, as illustrated in FIG. 6C, when the pressure decreasing period is excessively long (longer than a period TG in the figure), since the output signal of the OR circuit 502 is low level until the counter 501 counts up to the final digit, the signal f$$RF becomes high level. As described above, it is now possible to monitor the arithmetic operation result of the microcomputer 60 using the logic circuit illustrated in FIG. 6.

Detail Description Paragraph:
[0099] A logic circuit illustrated in FIG. 7A is a sequence monitoring logic circuit for monitoring the sequence of the data transmitted from the microcomputer 60. That is, since it is assumed that the serial signal transmitted from the microcomputer 60 is not transmitted accurately if the data having ID number A and the data having ID number B are not received alternately, the microcomputer 60 is assumed to be in the fault condition in this case.

Detail Description Paragraph:
[0106] Accordingly, outputs of the D type flop-flops 605 and 606 become low level and the signal fSQNG outputted from the AND circuit 607 becomes high level in order to detect a fault in the data transmission sequence of the microcomputer 60 from the signal fSQNG. As described above, it is possible to monitor the sequence of the microcomputer 60 using the logic circuit of FIG. 7A.

Detail Description Paragraph:
[0107] As described above, various monitoring operations, such as monitoring for a fault of the arithmetic operation result of interval of arithmetic operations of the microcomputer 60 and monitoring for the sequence of data transmitted from the microcomputer 60 can be made through the data communication from the microcomputer 60.

Detail Description Paragraph:
[0108] As described above, a fault of the microcomputer 60 can be monitored easily even if two microcomputers are not provided by monitoring whether the data

communication from the microcomputer 60 is executed surely or not or whether content of data transmitted is accurate or not through the data communication to the peripheral IC 70 from the microcomputer 60. Moreover, since various monitoring operations can be realized through data communication from the microcomputer 60, sufficient monitoring capability can be attained in comparison with the WD monitoring operation.

Detail Description Paragraph:
[0109] Therefore, a fault of the microcomputer 60 can be monitored easily and effectively based on the data communication to the peripheral IC 70 from the microcomputer 60 and moreover the microcomputer 60 can be monitored with a more low cost structure.

Detail Description Paragraph:
[0110] The monitoring result of the serial signal monitor unit 74 is transmitted to the drive inhibit signal generating unit 78 directly or when the signal notifying a fault of the microcomputer 60 continues for a predetermined period or for a plurality of times. Upon reception of this monitoring result, the drive inhibit signal generating unit 78 outputs the solenoid drive inhibit signal and motor drive inhibit signal.

Detail Description Paragraph:
[0113] In this embodiment, as an example of the two-way communication, the method of monitoring the wheel speed arithmetic operation conducted by the microcomputer 60 will be described. FIG. 8 illustrates an ECU for ABS control to be used to monitor the wheel speed arithmetic operations.

Detail Description Paragraph:
[0115] The period of the wheel speed signal inputted from the microcomputer 60 is measured and the result is converted to the wheel speed data for use as the control parameter of the system. On the other hand, the microcomputer 60 and the peripheral IC 70 execute the following processing to monitor the normal conversion to the wheel speed data of the microcomputer 60.

Detail Description Paragraph:
[0116] (1) The microcomputer 60 selects a channel (CH) of the wheel to be monitored. Moreover, it also inversely executes the arithmetic operation for a period of the wheel speed signal from the wheel speed data of the selected channel. The selected channel data and the inversely calculated period data are transmitted to the peripheral IC 70 from the serial communication unit 64.

Detail Description Paragraph:
[0120] As described above, it is also possible to monitor whether the period measurement and arithmetic operation of the wheel speed are executed accurately or not in both the peripheral IC 70 and microcomputer 60 by conducting the period measurement of wheel speed signal in both microcomputer 60 and peripheral IC 70.

Detail Description Paragraph:
[0121] In this embodiment, period measurement and wheel speed calculation of the wheel speed signal are described but it is also possible to monitor the signals other than the wheel speed signal when it varies periodically in the same manner in this embodiment.

Detail Description Paragraph:
[0125] Moreover, in the first embodiment, the one-way communication for data communication to the peripheral IC 70 from the microcomputer 60 is described and the two-way communication is also possible as described in the second embodiment. For example, it is also possible to transmit the result of monitoring operation in the serial signal monitor unit 74 to the microcomputer 60.

Detail Description Paragraph:
[0126] In addition, in the first embodiment, it has been described as to whether the calculation for ABS control is conducted normally or not. However, in the case of ECU used for the brake apparatus comprising a brake assisting function, it can also be monitored whether the microcomputer 60 normally executes the calculation for the brake assisting function or not. For example, for the structure illustrated in FIG. 1, the first embodiment can be applied to the ECU adapted to the brake apparatus comprising the piping for connecting the master cylinder 16 or the master reservoir and the inlet port sides of the pumps 45a, 45b and control valves between each port of the master cylinder and the dual-position valves 21 to 24.

Detail Description Paragraph:
[0127] FIG. 9A illustrates a logic circuit used to monitor whether the calculation for the brake assisting function is conducted normally or not. FIGS. 9B and 9C illustrate timing diagrams during the operation of this logic circuit.

Detail Description Paragraph:
[0130] On the other hand, when the brake assisting control is executed, an instantaneous braking is conducted under the ABS control condition and thereby the counter 804 starts the counting operation in the timing of rise of pulse of the signal Q14. Since the brake assisting control is executed, the signal PBA becomes high level but the signal fBA becomes low level and the counter 804 is reset because the vehicle usually stops if the brake assisting control is conducted for a certain period of time.

Detail Description Paragraph:
[0131] (2) For example, if the brake assisting control is not cancelled even when the vehicle stops, for example, with the brake assisting control and ABS control, the ABS control is still continued and therefore the counter 804 performs the counting operation in the timing of rise of pulse of the signal Q14. Moreover, since the brake assisting control is executed, the signal PBA becomes high level. Since the brake assisting control is not yet cancelled, the signal PBA is maintained in the high level and the counter 804 is not reset. Therefore continues the counting operation up to the final digit.

CLAIMS:

1. A method of monitoring a microcomputer in an electronic control unit comprising a microcomputer and a peripheral IC, the method comprising the steps of: transmitting data from the microcomputer to the peripheral IC; and monitoring a fault of the microcomputer by the peripheral IC based on the data received from the microcomputer.

2. The method as in claim 1, further comprising the steps of: transmitting data from the peripheral IC to the microcomputer; and monitoring faults of the microcomputer and the peripheral IC by the microcomputer based on the data received from the peripheral IC.

3. The method as in claim 1, further comprising the step of: monitoring an interval of data communication from the microcomputer by the peripheral IC.

4. The method as in claim 1, wherein: a plurality of data communications are performed to the peripheral IC from the microcomputer; and the monitoring step of the peripheral IC monitors a sequence of the plurality of data communications from the microcomputer.

9. A control unit comprising: a microcomputer; and a peripheral IC, wherein the microcomputer is constructed to transmit data to the peripheral IC, and wherein the peripheral IC is constructed to monitor a fault of the microcomputer based on the data received from the microcomputer.

10. The control unit as in claim 9, wherein: the peripheral IC is constructed to transmit data to the microcomputer; and the microcomputer is constructed to monitor the fault of the microcomputer based on the data received from the peripheral IC.

11. The control unit as in claim 9, wherein: the peripheral IC is constructed to monitor an interval of data communication from the microcomputer.

12. The control unit as in claim 9, wherein: the microcomputer is constructed to communicate a plurality of data to the peripheral IC; and the peripheral IC is constructed to monitor a sequence of the plurality of data from the microcomputer.

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